1. An architect decides to not have a branch predictor at all. What is the significance of this decision? How much slowdown to expect for what types of applications --- provide some estimate for the typical numbers of an out-of-order superscalar processor that we have studied in the course (mention the numbers that you use while justifying your answer).

2. Why do we need a return address stack? Can't a branch target buffer predict the return address too?

3. Explain how can a deadlock occur in a hyper-threaded (SMT) setting if we are not careful about designing our buffers? What is the mistake that can result in a deadlock situation?

4. Why would vectorization result in a speedup, when we already have an OOO superscalar processor? Provide the most important factors for this.